Signal-Flow Based Circuit Simulation

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The simulation of integrated circuits enables the verification of the correct functioning and provides important performance values prior to their fabrication. In particular the accurate but time-consuming circuit-level simulation plays a central role in the design process. Due to the ever increasing complexity of integrated circuits and the associated rise in computing time, there is a continuing need in efficient numerical methods for the solution of the resulting high-dimensional systems of differential and algebraic equations.

The standard approach to solve these systems can be split into two main steps: the computation of consistent initial conditions and the numerical integration with implicit one-step or multi-step methods. In this thesis, we develop different models of the signal flow of integrated circuits and propose graph-based methods to speed up the simulation exploiting information on the underlying network structure.

The determination of consistent initial values necessitates the solution of a system of nonlinear equations. In order to improve the convergence of the Newton–Raphson method, which is usually used to solve the system of equations, and thus to reduce the simulation time, we compute an appropriate starting point using an event-driven switch-level algorithm in combination with a model of the logic signal flow that is based on the partitioning into channel-connected and strongly connected components.

Another possibility to reduce the runtime is to exploit subsystems that are temporarily inactive during the transient simulation. We introduce a dependency graph which enables the prediction of the influence of signal changes and a splitting of the system into active and inactive subsystems. Based on this decomposition, we define signal-flow based Runge–Kutta methods which automatically identify inactive subsystems and skip the recomputation of these regions. This leads to a significantly reduced number of time-consuming function evaluations.